WHAT IS CLAIMED IS:

1. A method of verifying correct operation of a forward error correction decoder, comprising the steps of:

programmably selecting a desired number of errors for insertion into a plurality of data signals;

defining a plurality of code words of the data signals;

inserting into one of the data signals the desired number of errors using an error insertion circuit;

repeating said inserting step in an iterative fashion to insert into different data signals the desired number of errors wherein the errors are placed within the code words of the data signals at different location permutations for each data signal;

transmitting the data signals with the inserted errors to a receiver; and

determining that the data signals received at the receiver contain the inserted errors.

2. The method of Claim 1 wherein said repeating step cycles through all possible permutations of all the code word locations.

3. The method of Claim 1 wherein the error insertion circuit operates in one of a plurality of modes, including a short frame mode for shorter permutation cycles, and further comprising the steps of:

selecting the short frame mode for operation; and

in response to said selecting step, limiting said repeating step to cycle through less than all possible permutations of all the code word locations.

4. The method of Claim 1 wherein:

the data signal is a SONET data signal having nine rows; and

said repeating step results in the insertion of errors in 32 code words defined within each of the nine SONET rows.

5. The method of Claim 1 wherein said repeating step stops after one permutation cycle in response to the further step of programming the error insertion circuit for single cycle operation.

6. The method of Claim 1 wherein said determining step includes the step of examining an error accumulator count in the receiver to match a number of accumulated errors with the number of inserted errors.

7. The method of Claim 6 wherein said examining step matches the number of accumulated errors with the number of inserted errors using a modulo function.

8. The method of Claim 1 wherein:

the error insertion circuit includes an error mask for selectively preventing insertion of one or more of the errors; and

said repeating step is limited to inserting errors in selected code words based on the error mask.

9. The method of Claim 1 wherein said repeating step includes the step of tracking the location of a current code word in which an error is being inserted.

10. The method of Claim 9 wherein said tracking step includes the step of incrementing one or more registers in a location counter having at least first, second, and third registers, the first register corresponding to a column location, the second register corresponding to an index location, and the third register corresponding to a byte location.

11. A method of injecting a plurality of errors into a SONET data stream, comprising the steps of:

programming an error insertion circuit to select a desired number of errors for insertion into a plurality of successive SONET data signals each having a plurality of rows;

defining a plurality of forward error correction (FEC) code words within each of the rows of the SONET data signals;

inserting the desired number of errors into a first one of the SONET data signals at a first code word permutation location, using the error insertion circuit;

tracking the first code word permutation location in response to said step of inserting the desired number of errors into the first SONET data signal; and

inserting the desired number of errors into a second one of the SONET data signals at a second code word permutation location, using the error insertion circuit, and in response to said tracking step.

12. The method of Claim 11 further comprising the step of programming the error insertion circuit for single cycle operation.

13. The method of Claim 11 further comprising the step of programming the error insertion circuit for short frame mode operation.

14. The method of Claim 11 wherein said tracking step includes the step of incrementing one or more registers in a location counter having at least first, second, and third registers, the first register corresponding to a SONET column location, the second register corresponding to an index location, and the third register corresponding to a byte location, the index and byte locations together representing a SONET byte location.

15. The method of Claim 11 wherein said inserting steps occur after the further step of scrambling the SONET data signals.

16. An error injection circuit comprising:

means for selectively programming a desired number of errors for insertion into a plurality of data signals;

means for defining a plurality of code words of the data signals; and

means for repeatedly inserting the desired number of errors into different ones of the data signals at different code word permutation locations.

17. The error injection circuit of Claim 16 wherein said inserting means cycles through all possible permutations of all the code word locations.

18. The error injection circuit of Claim 16 further comprising means for selecting a short frame mode of operation, wherein said inserting means limits insertion of the errors to cycle through less than all possible permutations of all the code word locations when the short frame mode of operation is selected.

19. The error injection circuit of Claim 16 wherein:
the data signal is a SONET data signal having nine rows; and
said inserting means inserts errors in 32 code words defined within each of the nine SONET rows.

20. The error injection circuit of Claim 16 further comprising means for selecting single cycle operation, wherein said inserting means stops inserting errors after one permutation cycle when the single cycle operation is selected.

21. The error injection circuit of Claim 16 further comprising error mask means for selectively preventing insertion of one or more of the errors, wherein said inserting means inserts errors in selected code words based on said error mask means.

22. The error injection circuit of Claim 16 wherein said insertion means includes means for tracking the location of a current code word in which an error is being inserted.

23. The error injection circuit of Claim 16 wherein said tracking means increments one or more registers in a location counter having at least first, second, and third registers, the first register corresponding to a column location, the second register corresponding to an index location, and the third register corresponding to a byte location.

24. An OC-192 input/output card comprising:
four OC-48 processors; and

an OC-192 front-end application-specific integrated circuit (ASIC) connected to said four OC-48 processors, said OC-192 front-end ASIC including

a transmitter having means for interleaving four OC-48 signals to create an OC-192 signal, and means for encoding forward error correction (FEC) codes in each of the four OC-48 signals,

a receiver having means for de-interleaving an OC-192 signal to create four OC-48 signals, and means for decoding FEC codes in the OC-192 signal, and

means for verifying correct operation of said encoding means and said decoding means.

25. The OC-192 input/output card of Claim 24 wherein said verifying means includes:

means for selectively programming a desired number of errors for insertion into a plurality of successive SONET data signals;

means for defining a plurality of FEC code words of the SONET data signals;

means for repeatedly inserting the desired number of errors into different ones of the SONET data signals at different code word permutation locations;

means for routing the SONET data signals with the inserted errors from said transmitter to said receiver; and

means for determining that the SONET data signals received at said receiver contain the inserted errors.

26. The OC-192 input/output card of Claim 25 wherein said inserting means cycles through all possible permutations of all the FEC code word locations.

27. The OC-192 input/output card of Claim 25 further comprising means for selecting a short frame mode of operation, wherein said inserting means limits insertion of the errors to cycle through less than all possible permutations of all the code word locations when the short frame mode of operation is selected.

28. The OC-192 input/output card of Claim 25 further comprising means for selecting single cycle operation, wherein said inserting means stops inserting errors after one permutation cycle when the single cycle operation is selected.

29. The OC-192 input/output card of Claim 25 further comprising error mask means for selectively preventing insertion of one or more of the errors, wherein said inserting means inserts errors in selected code words based on said error mask means.

30. The OC-192 input/output card of Claim 25 wherein said insertion means includes means for tracking the location of a current code word in which an error is being inserted.

31. The OC-192 input/output card of Claim 24 wherein said programming means allows from one to four errors to be inserted in a given SONET data signal.

32. The OC-192 input/output card of Claim 24 wherein said encoding means and said decoding means use a triple-error correcting Bose-Chaudhuri-Hocquenghem (BCH) code.

33. The OC-192 input/output card of Claim 25 wherein said determining means includes an error accumulator located in said receiver, and means for examining an error accumulator count of the error accumulator to match a number of accumulated errors with the number of inserted errors.

34. The OC-192 input/output card of Claim 30 wherein said tracking means increments one or more registers in a location counter having at least first, second, and third registers, the first register corresponding to a SONET column location, the second register corresponding to an index location, and the third register corresponding to a byte location, the index and byte locations together representing a SONET byte location.

35. The OC-192 input/output card of Claim 34 wherein said tracking means contains 10 location counters, including:

a first location counter for tracking a location of a first error bit;

second and third location counters nested together for tracking a location of a second error bit;

fourth, fifth and sixth location counters nested together for tracking a location of a third error bit; and

seventh, eighth and ninth location counters nested together for tracking a location of a fourth error bit.

36. The OC-192 input/output card of Claim 33 wherein said error accumulator accumulates both corrected errors and uncorrectable errors.

37. An error injection circuit comprising:

an error selection interface which programs a desired number of errors for insertion into a plurality of data signals;

an encoding circuit which defines a plurality of code words of the data signals; and

a location counter which increments through a plurality of locations in each of the code words and inserts the desired number of errors into different ones of the data signals at different code word permutation locations.

38. The error injection circuit of Claim 37 wherein said location counter means cycles through all possible permutations of all the code word locations.

39. The error injection circuit of Claim 37 wherein:

the data signal is a SONET data signal having nine rows; and

said inserting means inserts errors in 32 code words defined within each of the nine SONET rows.

40. The error injection circuit of Claim 37 further comprising an error mask which selectively prevents insertion of one or more of the errors in selected code words